

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

- 5 Claim 1 (currently amended) A semiconductor wafer comprising:
a substrate with a first region, a second region, and a third region
horizontally defined on the surface thereof;~~and~~
a capacitor disposed on the substrate, the capacitor further
comprising:
10 a first electrode disposed in the first region and the third region
on the substrate;
a first isolation layer disposed on the first electrode, the first
isolation layer covering a portion of the first electrode and
the substrate; and
15 a second electrode disposed on the first isolation layer, the
second electrode covering the first electrode in the third
region and covering the substrate in the second region;
a second isolation layer covering the capacitor and the substrate; and
a first contact plug located only in the second isolation layer and
20 electrically connected to the first electrode.

Claim 2 (cancelled)

Claim 3 (cancelled)

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Claim 4 (currently amended) The semiconductor wafer of claim [[3]]1
wherein the first contact plug is located in the first region.

Claim 5 (currently amended) The semiconductor wafer of claim ~~[[2]]~~1
wherein the capacitor further comprises a second contact plug located in
the second isolation layer and electrically connected to the second
5 electrode.

Claim 6 (original) The semiconductor wafer of claim 5 wherein the second
contact plug is located in the second region or the third region.

10 Claim 7 (original) The semiconductor wafer of claim 1 wherein the
semiconductor wafer further comprises a field oxide layer located beneath
the first electrode.

Claim 8 (original) The semiconductor wafer of claim 1 wherein the first
15 electrode comprises a polysilicon layer or a doped polysilicon layer.

Claim 9 (original) The semiconductor wafer of claim 1 wherein the second
electrode comprises a polysilicon layer or a doped polysilicon layer.

20 Claim 10 (original) The semiconductor wafer of claim 1 wherein the first
isolation layer comprises a silicon oxide layer or a silicon nitride layer.

Claim 11 (currently amended) A capacitor disposed on a substrate, the
substrate having a first region, a second region, and a third region
25 horizontally defined on the surface thereof, the capacitor comprising:

a first polysilicon layer disposed in the first region and the third
region on the substrate;

a dielectric layer covering a portion of the first polysilicon layer_and

the substrate; [[and]]

a second polysilicon layer disposed on the dielectric layer, the second polysilicon layer covering the first polysilicon layer in the third region and covering the substrate in the second region[.];

5 an isolation layer covering the first polysilicon layer and the second polysilicon layer; and

a first contact plug located only in the isolation layer and electrically connected to the first polysilicon layer.

10 Claim 12 (cancelled)

Claim 13 (currently amended) The capacitor of claim [[12]]11 wherein the first contact plug is located in the first region.

15 Claim 14 (original) The capacitor of claim 11 wherein the capacitor further comprises a second contact plug electrically connected to the second polysilicon layer.

20 Claim 15 (original) The capacitor of claim 14 wherein the second contact plug is located in the second region or the third region.

Claim 16 (original) The capacitor of claim 11 wherein the capacitor further comprises a field oxide layer located under the first polysilicon layer.